Design Validation and Test Challenges in the Fabless SOC Business

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Agenda

- Planning
- Staffing
- Libraries
- Toolsets
- Relationships
Planning the Device Flow

- Design
- 1st Silicon Test
- Production
- Customer
Planning Considerations

- Product concept
- Architecture
- Technology choice
- Design approach
- Test approach
- Manufacturing approach
Planning Considerations

- Product concept
- Architecture
- Design approach
- Test approach
- Technology choice
- Manufacturing approach
- Test strategy approach
- Validation / characterization approach
- Maintenance approach
The “Standard Model”

- Design the device
  - with foundry-approved tools
- Fabricate the device
- Probe with customer-provided vectors
- Package good devices
- Test with customer-provided vectors
- Ship
Failure to allow for iteration can lead to a disaster.
Using the Standard Model

- Problem - what are the DPM’s?
- Raw yields from the fab process:
  - Routine digital device - 75-95%
  - Leading-edge digital device - 60-80%
  - Complex mixed-signal device - 25-65%
  - Tough SOC-type device - 5-30%
- **Testing** is an enabling technology
Today, testing is the path
But which tests? How many tests?
What is your tolerable DPM Level?
  – Safety-critical - zero defects
  – Speak-and-spell - 20,000 DPM
Tests, test coverage, and escapes
Types of test and defects

• Many different types of tests
  – IDDQ
  – Scan@probe (static / transition / delay)
  – Scan@package (static / transition / delay)
  – BIST (w-w/o MISR, etc)
  – FT@probe (slow / at-speed)
  – FT@package (slow / at-speed)

• Analog functionality tests
  – Appropriate test for any analog function
Test Coverage and Escapes

Sematech Study S121 (1997)
- Scan: 99.7% fault coverage
- FUNC: 52% fault coverage
- IDDQ: 1478 “non-operational” (of 1764 total IDDQ failures)
Test and Validation

• Wafer Probe
  – Earliest and least expensive opportunity to check for device functionality

• Packaged Device Test
  – Eliminate all faulty devices from the flow

• Device Validation testing
  – Both Design and Test
Wafer Probing

- **Objective**
  - Identify “almost all” of the defective die, to minimize wasted packages / MCM’s

- **Strategic approach**
  - Apply “high-enough” coverage test to as many die in parallel as possible

- **Tactical approaches**
  - Scan, BIST, IDDQ, some functional tests
Packaged device testing

- **Objective**
  - Achieve target DPM levels

- **Strategic approach**
  - Apply tests which identify defects not detected at wafer or imposed by packaging

- **Tactical approaches**
  - Repeat wafer-probe tests
  - Full functional test, systest, delay test
Device validation

• Objective
  – Assure final design realizes all objectives
• Strategic approach
  – Execute functional validation vectors
  – Run device in example final system
• Tactical approaches
  – At-Speed functional test, scan-based functional exercises, systest
Device Characterization

• Objective
  – Establish operating margins

• Strategic approach
  – Apply tests using equipment which can execute shmoos, searches, and sweeps

• Tactical approaches
  – Full functional test, extended-range system tests
To Probe or not to Probe?

Savings per Part

Package Cost / Probe Cost per device
Yield vs maturity vs complexity

Yield (%)

Relative Device Complexity

Process Maturity (Quarters)
Other Wafer Probe Issues

• Wafer probe tooling costs
  – Probe fixture development
  – Probe test development
  – Probe test debug
  – Lead time - especially for the first run

• Diagnosis and failure analysis
  – Repair tools apply more easily to chips
  – Chip thinning is easier than wafer thinning
The Distributed Test Strategy

- Defect types
  - some do not have good fault models
- Choose tests that find defects
- Apply tests in appropriate order
  - which depends on experience
- Discard tests which find no defects
  - which depends on LOTS of experience!
An IC Test Flow Model
Yield/DPM Goals

25-97% Wafer Fab

95-98% Probe Test

98-99.8% Package Test

99.8% (2K DPM) Burn-in Test

100-500 DPM System Test

SHIP
Test Cell Capital Cost / UPH

- Wafer Fab
- Probe Test
- Package
- Package Test
- Burn-in Test
- System Test
- SHIP

- $1,800K/1200
- $180K/45
- N/A
### Distributed Test Strategies

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<th>Subassy</th>
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The SOC Device Project Plan

- Don’t leave out the iterations
- Provide for all the testing you will need
- Anticipate the unknowns
- Concentrate on VALIDATION
- Allow for CHARACTERIZATION
Agenda

- Planning
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- Relationships
Many tasks are involved

- Test Strategy Definition
- Test Engineering
- Test Time Reduction
- Yield Enhancement
- Failure Analysis
- Field Return Statistics
Who does what when?

- Test Strategy Definition
- Test Engineering
- Test Time Reduction
- Yield Enhancement
- Failure Analysis
- Field Return Statistics

Who has incentive?
Incentive: Fabless? Foundry?

Fabless

Design

1st Silicon Test

Production

Customer

Design Diagnostic & Repair

Yield Analysis & Improvement

Failure Analysis

Interaction

?
Conflict Example

- Yield Improvement is not a benefit for Fabless if “price per good die” is predetermined.
- Test Time Reduction is not a benefit for Test House if “price per second” is predetermined.

Cost benefits must be equally distributed to encourage good collaboration.
Outsourcing?

- Characterization and Test needs design knowledge, but close to manufacturing.
  - Some fablesses own the characterization and test capability (inc. capital equipment), but not everybody can afford it.
  - Why not outsourcing?
Agenda

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Cell Libraries

- Logic cells and testable design
  - Testable design means more than scan
- Complex cores and their testability
  - Ability to apply core tests is critical
- Redundancy, Reliability, Repairability
  - Reconfigurable Logic Areas - FPGA
  - Multiple Redundant Implementations
  - Self-checking and on-line testing
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Technology and Tools

- Software tools
  - CAE, synthesis, layout, statistics
- Hardware tools
  - Testers
  - Verification tools
  - Diagnostic tools
  - Repair tools
The software tools situation

- CAE has come a lo-o-o-ong way!
  - Scan insertion, BIST insertion, synthesis
  - Still waiting for layout-driven synthesis with testpoint/scan insertion included
- Fault models are a generation behind
  - Coupling defects
  - Ground bounce
  - Marginal $V_T$
Coupling Problems

\[ T_D = 0.8 \text{ ns} \]

\[ T_D = 0.3 \text{ ns} \]

\[ T_D = 3 \text{ ns} \]

<table>
<thead>
<tr>
<th>PRPG’s will not do this!</th>
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<tbody>
<tr>
<td>Can ATPG’s?</td>
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\[ \text{bus} \]

| 00000000 |
| 11111111 |
| 00000000 |
| 00001000 |
| 11110111 |
| 00001000 |

\[ V_T \]

result

\[ T_D = 0.3 \text{ ns} \]

\[ T_D = 3 \text{ ns} \]
Process Shrinks

0.5µm -- 5 million transistors

0.1µm -- 250 million transistors

A Transistor

Not Much Thinner!

A Transistor

Aluminum Conductors
4-5 Levels

Oxide Dielectric

Copper Conductors
(8 Levels)

Tungsten Plugs

Low-K Dielectric

Copper Plugs

0.1µm -- 0.5µm

-- 250 million transistors

-- 5 million transistors

-- 250 million transistors

-- 5 million transistors
Pareto of Defects - 350 nm

- Unknown
- BridgeM1-2
- Via break
- Bridge M2
- Bridge M4
- Break trans
- Bridge Poly M1
- Bridge M3
- Bridge M1-3
- Bridge poly M2
- Bridge M3-4
- Open Poly
- Open Contact
- Bridge M1
- Unknown Br
- Break M3
- Bridge Poly M2
- Break M2
- Bridge M3-4
- Break M1
- Bridge Poly M4
- Bridge Poly

- Unknown
- Open Vias
- Metal Breaks
- Bridges (resistive)

Open defects are not modeled well at all

Open Poly
Open Contact

100 nm - a new distribution
The hardware tools situation

• Wafer level characterization becomes more important.
  – Margin analysis is critical for yield.
• Front-side probing becomes more challenging.
  – Back side probing and “design for debug”
• General purpose tester or focused tester?
Wafer level characterization

- Eg. AC timing Analysis using EB tester.

IDS10000cs
Back-side probing technique

- Laser probing by IDS2500
- Photo Emission by PICA

IDS2500

PICA image
Focused Tester

• General purpose (or all-in-one) testers are common.
  – Not necessarily efficient for a particular test function.
• Focused Tester would be economical for strategic test flow.
  – Burn-in testers and DFT testers are good examples.
Agenda

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Filling the gap
A strong partnership can enable good communication between Foundry and Fabless.

Outsourcing is one means to create a bridging partnership that can avoid the conflicts between Foundry and Fabless.
Summary

• There is no “magic bullet” for test
• Test/validation requirements will evolve
• Equipment will evolve correspondingly
• CAE will also have to evolve
• A test, validation, and characterization outsourcing relationship can make the critical difference for success