At-Speed Structural Test

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Abstract

Structural test can address only stuck-at faults unless some dynamic capability is included. The dynamic capability required starts with two-vector launch-capture delay tests, but evolves rapidly to include gated clock bursts, perhaps synchronized with primary I/O's. This implies an at-speed structural test architecture which incorporates many of the capabilities of functional test systems.

1 Introduction

Qualifying complex IC's by verifying their structural integrity, rather than checking their functional performance, is becoming more popular. This test process is called "structural testing".

The simplest structural tester is one which merely investigates the static logical structure of an IC through a JTAG 1149.1 Boundary Scan port[1]. This is possible if the IC is implemented with the appropriate private JTAG instructions and uses full scan design[2]. Such a tester is little more than a few power supplies, a device fixturing arrangement, three digital input drivers, one digital output receiver, and a computer. The only hardware requirement the computer must satisfy is that it has enough program memory and disk storage to handle all the test data. If the power supplies have good current monitoring capability, such a tester could also add IDDQ measurement to its structural analysis repertoire.

Such a tester unfortunately does not address the dynamics of the device, which are becoming more important as device geometries continue their dramatic approach to molecular scale.

In this paper, we consider implementation requirements for a structural tester whose objectives are to qualify high-performance devices and help determine where and why the inevitable failures occur.

2 Why Test?

The reasons for testing are
- to establish whether performance requirements are met
- when not met, to assist in determining why not

If there is no risk about meeting a requirement, there is no need to test for it. On the other hand, if any performance requirements are at risk in the manufacturing process, a test strategy which does not address the risk is incomplete.

Requirements are based on performance specifications. They may be at risk due to marginal design or process variations, or they may be at risk due to defects introduced in the normal flow of manufacture. "Marginal design" in this context is a benign phrase. It means design which depends on test screening to establish performance margins. Process variations produce performance variations, which produce opportunities for revenue enhancement by speed-bin[ing][3].

Tests aimed at maintaining process quality cannot address margin impairment due to normal process variation. Nor can they certify acceptable product that may result even when the process runs slightly out of tolerance. Therefore, if normal process variations can lead to unacceptably slow devices, then device speed performance must be verified.

Tests aimed at detecting manufacturing defects cannot determine whether the defect renders the product unsuitable, as Davidson pointed out (with specific reference to IDDQ tests) [4].

Assistance in fault location requires testing that delivers information about the location of the fault. This issue becomes ever more severe, as the devices tested become ever more complex.

3 Test Techniques and Results

Effectiveness of different test techniques has often been studied - for example see [5] and [6]. The techniques used in these two cases were IDDQ, functional tests, scan-based stuck-at tests, and (in [6]) scan-based delay tests. In these studies, a substantial number of faults are IDDQ-only - over 30%(1358 of 4349) in the former and over 50% (1463 of 2892) in the latter. These numbers are upper bounds on potential IDDQ yield loss.

These studies do not reflect deep-submicron technology impacts. Both observe that IDDQ threshold determination is uncertain. It becomes even more uncertain as device geometries and operating voltages decrease[7] - hence IDDQ yield loss upper bounds will increase unless the IDDQ testing pro-
cess itself improves significantly in resolution and reliability. Progress is being made in this area, however[8].

These studies also point out that delay faults are not well correlated with IDDQ faults. In [5], 10 of 21 faults detected by delay tests and not by static functional or scan tests were not IDDQ failures.

Finally, in both studies a small but significant number of faults was detected ONLY by the functional tests. This fact was particularly striking in [6], because the stuck-at fault coverage of the functional test was only 57% - and furthermore, it was only a low-speed functional test. Devices which fail functional tests, unlike IDDQ failing devices, are defective devices in that they do not meet operating requirements.

The conclusion one draws from these studies is that scan-supported at-speed functional testing is required.

Scan-supported tests are favored for fault isolation because they can localize failures to within a few devices. Scan-supported delay fault testing has a similar failure resolving power.

Recently, failure location by observing fault-induced radiation has shown promise, but it is of course limited to failure modes in which the fault modulates the radiation that is emitted[9]. Time-based faults were shown to be observable using this technique. In order to generate these symptoms, the authors noted that at-speed electrical testing was used.

Deep-submicron technology has additional, more direct impact on device timing. As the interconnect gets denser and denser, the effects of electrical interaction in the interconnect get worse and worse[10]. Timing paths have been shown to be poorly correlated with overall device performance[12].

4 At-Speed vs Static Structural Test

Given the limited visibility of complex devices, we quickly realize that DFT will become more widely accepted. Whether this DFT incorporates BIST or simply scan chains, it will become an important part of any complex device design.

We will now distinguish two classes of structural test systems - at-speed and static.

We will call a tester which exercises a subset of device pins, relying exclusively on scan paths or BIST activation supplemented by an internal clock generator (with, perhaps, IDDQ measure capability) for assuring device structural integrity a "static structural test system". This definition includes systems with clock reference for an internal PLL.

We will call a tester which is capable of driving a device at its rated speed, depending primarily on internal state as developed by scan or BIST, but supplying any required primary I/O’s or clock signals to the device, an "at-speed structural tester". It is distinguished from an at-speed functional tester by the fact that the primary inputs are not necessarily driven at speed and that synchronous evaluation of the primary outputs is not required for the test.

With this definition, one realizes that an at-speed functional test system with adequate pattern memory is a superset of a structural test system. Any test that can be implemented on either a static or a dynamic structural tester can be implemented on a functional tester with adequate pattern memory. The converse is not true.

Without explicit internal state control and initialization capability designed into a part, as is done by scan chains, full functional test and effective failure analysis have become extremely difficult.

5 Launch-Capture Testing

Launch-capture testing for delay fault detection and path speed analysis has proved to be very fruitful. Launch-capture tests, also called "two-vector tests", are an extension of static structural test where a two-cycle clock burst is provided. The scanned-in pattern is specially configured to establish a state transition in an internal combinatoric circuit at the first cycle of the clock, and then to capture that transition on the second cycle. This is shown in the following figure.
The double clock is launched on the F - T transition of the signal CLKE. The five 100E196 programmable delay lines are used to time the four edges of the two clock pulses required for launching the state change and capturing the result. The quad DAC provides resolution of order of a picosecond to each of the four edge placements. With careful construction, this circuit can be used to generate two cycles of a clock ranging in period from less than 200 MHz to over 1 GHz. An oscilloscope must be used to calibrate the clock edge alignment; however, the user must carefully take into account the error inherent in such a calibration process[14].

This circuitry does not extend conveniently beyond two clock cycles. As a consequence, for full at-speed structural testing, more clocking capability is required. Many high-performance designs use only a partial scan analysis structure, and these designs necessarily will require more cycles in their clock bursts. In addition, BIST structures frequently require hundreds or thousands of clock cycles for each test sequence.

6 System Architecture

Logically testing a digital device requires the ability to establish an appropriate starting state for the DUT, the ability to generate the appropriate test patterns, the ability to apply them to the DUT, and the ability to evaluate the response of the DUT to the patterns. This set of abilities is exhibited in the following utterly simplified block diagram.

This figure clearly recognizes that initializing a device must necessarily rely upon activity on the device input pins, which activity may range from a simple RESET signal to a PLL initialization loop followed by a full scan-in of a target initial state or a BIST initialization.

The stimulus pattern therefore includes both the activity involved in establishing the starting state and the activity involved in driving the device through the state-sequence transformation required by the test.

If there is a clock burst of more than two cycles duration, then the device primary inputs may become involved in the state-space transformation - particularly for devices with limited BIST. Certainly, the primary inputs must be held to specific selected logic states; more generally, they will change as required by the test sequence being implemented. These changes must be synchronized with the input clock, and they must take place satisfying device setup and hold timing requirements, or the required test will not be executed.

The response pattern analysis includes checking the expected activity at the outputs as a result of the sequence of states through which the DUT passes, as well as checking the internal state to the extent that it can be determined by scanning it out or evaluating signature or other BIST register contents.

The key requirement on this kind of tester is that it be able to apply appropriate event sequences on all device pins with acceptable timing accuracy[11].

The above test sequence is simply summarized:

- establish the starting condition
- drive the device through the test sequence
- evaluate the resulting condition

The second step is key. This step potentially incorporates both at-speed application of stored patterns to the primary I/O's of the DUT and appropriately timed and precisely denumerated clock bursts. Clock burst generation is discussed further below.

How many scan chains are there going to be? How much scan memory? Is scan memory separate
from pattern memory? These are key questions, and by now the answer to them has become clear.

The number of scan chains affects the device test time, and consequently the more the better. With many scan chains, scan memory becomes identical to pattern memory - there is no substantial reason to distinguish one from the other. Hence, pattern memory must be deep enough to accommodate the scan requirement. Fortunately, large memory devices are available which can supply ample pattern memory per pin at reasonable cost.

7 At-speed Structural Test Requirements

In the following subsections, we consider the requirements for:

- input timing accuracy
- input timing accuracy for gated clocks
- input pattern generation
- result evaluation

that at-speed structural test must satisfy.

7.1 Input Timing Accuracy

With modern high-performance microprocessors, internal circuitry is no longer limited to the speeds attainable at the I/O boundary. Internal clocks are running three, four, five, or more times as fast as external clocks. However, to the extent that structural tests depend on inputs on primary I/O’s, the actual accuracy required of transitions on the primary I/O’s can be limited by bus clock speeds.

If internal clocks are running faster than bus clocks, then it can become important to verify that the input data are properly received no matter which internal clock phase they meet. Imposing this requirement on primary I/O’s dramatically increases the timing accuracy requirement, and may make the earlier distinction between at-speed structural testing and at-speed functional testing academic. A structural tester will depend on scan input for this purpose.

The timing accuracy required on a set of scan inputs or outputs is obviously not as demanding as that required for speed-grading. Again, the only need is to satisfy the input register setup and hold time requirements, and to strobe during the time the output is stable.

It is this latter that most likely limits the scan data rates. Process variation and device dynamics will affect the clock-out delay times; if these effects amount to a nanosecond or so, then scan-out rates above 500 MHz will be somewhat difficult to measure reliably.

7.2 Input Timing Accuracy for Gated Clocks

Given scan-based DFT, with adequate device internal state establishment and analysis capability, internal failures can be detected and properly isolated simply by applying patterns and then evaluating the resulting internal state. To do this, however, the internal clock must be driven by the test equipment with explicit control over the rate and number of cycles applied. The following figure exhibits this concept.

This test process allows us to study the effects of a clock burst which will execute a number of cycles. It will clearly compress the overall test time. Perhaps more importantly, it will improve the accuracy and quality of the dynamic portion of the test.

It is important to realize that the device itself must provide clock inputs which will run at target internal clock speeds, and it must be able to run in PLL-bypass mode.

Generating bursts of clocks at and above a gigahertz is particularly challenging, given the dynamics of the clock signal path to the device being tested.

There is an additional issue, as well. Clock trees are generally designed for continuous clocking (as by an internal PLL, for example). However, when a large internal clock tree is stimulated by a short clock burst, significant phase errors are introduced by the dynamics of the device clock tree itself. As a consequence, the relationship between register transfers under short bursts and those under continuous clocking is problematic. It is likely that clock bursts may need some kind of precharge - perhaps a few clock cycles at 20% below target speed - in order to prevent false failures due to short-clocking on the first cycle. Alternatively, a first-cycle adjustment to allow for clock tree dynamics may be required.

Internal clocks in complex devices are currently exceeding 1 GHz; consequently, clock timing accuracy should be +/- 30 ps edge to edge.

Recently, internal clock generators with missing cycle and double-cycle capability have been introduced. These core clock bursters assume no phase distortion, and are ill-equipped to correct for it. However, they have been shown to be effective for identification of significant delay faults, as well as for some speed-grading.

7.3 Input Pattern Generation

Input pattern generation presents three very distinct tasks. Recall the test requirement:

- establish the starting condition
- drive the device through the test sequence
- evaluate the resulting condition

To establish the starting condition, we must bring the entire circuit under test into a particular well-de-
As noted earlier, the accuracy requirement on the edge-to-edge timing of the tester channels driving the device clock pins can be much higher than that on the data pins. Note that the actual primary input pin activity need not be particularly fast, even with the accuracy requirement - and indeed it need not even activate all pins.

Whether all pins are active or not, or how rapidly they need to change, will vary from device to device and from test sequence to test sequence on any device. Both input structures and output structures on modern highly complex devices are fairly robust against process defects - and as noted above there is no need to test for failures which will not occur. Further, a few vectors of JTAG boundary scan can resolve all questions about the integrity of any inactive I/O’s, whether they are actually probed or not.

### 7.4 Response Measurement

As noted above, the structural determination of the device response simply requires logging the output scan chains. If these scan chains include signatures based on activity during a pattern burst, then the actual device activity on its output pins during the pattern burst is probably not important to the test. Indeed, for the purposes of either at-speed or static structural test there is no obvious need to observe the device primary output pins at all.

Outputs will normally be generated during this pattern burst period, and strobing the primary outputs for additional failure detection and fault diagnosis may be worth while.

Device primary output measurement requires strobing within a window defined by the clock period and the dynamics of the clock tree and the device output structure. As output timing varies with device process variance, temperature, and internal dynamics, this window can get to be fairly small. Therefore, timing accuracy, resolution, and flexibility required to strobe device primary outputs during these dynamic tests become substantially equivalent to that of at-speed functional test. At-speed structural testers in general will not depend on measurements of device primary outputs.

### 7.5 Architectural Considerations

Two issues in scan chain application must be considered:

- the amount of scan memory required
- the time required to execute the tests

How much scan memory is required? The relation is easy to establish - number of registers times number of registers in the longest chain times number of test steps for which scan-in or scan-out is required. If two-vector tests are used throughout, the last term in this equation can get to be horrendously large. As noted above, it can be reduced dramatically, somewhat at the expense of test generation time, by using pattern bursts, or at the expense of device design time and area overhead by using sophisticated device-dependent BIST structures.

As devices become more and more complex, the number of clock cycles required to sensitize and detect deeply nested faults gets larger and larger. The number of cycles required for scan chain initialization also gets larger, of course. However, if the device has a large number of independent scan chains (as, for example, by overloading primary input or output pins) scan chain initialization can become much less time-consuming than functional initialization.

Distributing the scan data over a large number of pins does not change the amount of memory required, but it changes the distribution and dramatically affects test time. The more scan chains there are, the faster the device can be tested - and the speedup is almost linear in chain count.

Furthermore, the scan data rate directly affects the test time. For two-vector full-scan tests, for example, the test time required with 400 MHz scan chains is hardly more than half that required when 200 MHz scan chains are used. Consequently, it is economically justifiable to pay 75% more for a test system that runs scan chains twice as fast, other things being equal.

### 8 Conclusion

In this paper, we have defined at-speed structural testing and described the architectural requirements for it. We also showed that the demanding timing measurements needed by modern devices can be addressed by properly designed and configured at-speed structural test systems, provided device clock trees are properly accounted for. Finally, we showed that, for devices whose expected performance is limited by process parameters, any test strategy that does not incorporate some form of at-speed testing is incomplete.

### References


